

UDC 681.322

**S.V. Lenkov, Doctor of technical sciences, professor,  
Y.A. Gunchenko, Doctor of technical sciences, associate professor,  
V.V. Savenchuk.**

## **DESIGN AND ANALYSIS OF CPU DESIGNS.**

*In this paper the principles of jam protected CPU design for modern computing systems are analyzed. Functioning and features of modernization for three CPU designs are described, their advantages and disadvantages are shown, dependences of work's speed (number of executed instructions) from probability of an error of calculations are given.*

**Keywords:** *processor, CPU design , signature, computing system.*

### **Introduction**

In modern computer systems, special purpose often acute problem of reliability. The are three types of tasks: improvement of reliability of data storage; - improvement of reliability of data transfer; improvement of reliability (reliability). The first and second types are aimed at detecting and fixing errors that occur when sending or storing data, and the basis of their decisions have a mathematical or physical character. There are many different ways to improve the reliability of data storage and transfer: use control (bits) Hamming code parity and other more complex codes. The decision also tasks the third type is associated with changes in the architecture of the computing device and the system at large.

### **Statement of the problem**

The need to improve the reliability of the calculations the most strongly felt in distributed computing, as well as the building of distributed control systems of various purpose. This was made possible thanks to a sufficient level of development of modern computer networks that allow for the use of a large number of remote computers. Existing approaches to building distributed systems of data processing in the network resources are built as an add-in technology on standard operating systems. The result is multi-layer software systems, which require complex administration. Examples of specialized systems that give a picture of the extent and scope of the distributed systems of data processing, are given in table 1.

## The purpose of the work

Thus, the problem of increasing the reliability of calculations at this point is relevant, and its solutions are in demand. Improvement of reliability calculation by changing the architecture can be both indirect (for example, when building a systolic computation systems, where each compute element solves similar tasks, to simplify its structure, but in a more simple structure more easily achieved the required dependability), and directly affect the reliability of the calculations. Let's look at an example of such a system is the CPU [2, 3].

## Main Part

**Comparison of architectures.** Thus, error control unit calculates the result correct if its signature matches the one of the previous two signatures. Define the probability of obtaining a result of wrong (incorrect signature) for three of processor architectures. Take the chance of getting an erroneous signature on each loop (step) equiprobable and equal to  $r$ , then the probability of getting the correct signature  $q = 1-p$  command less than two cycle cannot be in any of the three architectures. Relabel  $P_i(n)$  the probability of execution of a command on the  $n$ -th step of the 1st architecture. The command less than 2 steps in the architectures not possible because  $P_i(n) = 0$  if  $n < 2$  for any  $i$ ; also note that the  $P(2) = q^2$  for any architecture, because the differences in them are observed only when an error is detected, and the adoption of the result on the second step of her absence.

$$P_1(n=2k) = q^2(1-qq)^{k-1}.$$

Consider the original architecture 1. The result is accepted only at even the number of cycles (2, 4, 6, ...). For each pair of loops (1 and 2, 3 and 4, ...) a chance to take the  $q^2$  result is therefore a chance to reject the result is  $(1-q^2)$ . To apply the result to the  $n$ -th step should be to: the result of the last two) were correct; b) result has not been adopted at the previous  $(n-2)$ , which was rejected by the  $(n-2)/2$  times. Thus:  $P_1(n = 2k) = q^2 (1-qq)^{k-1}$ .

$$P_2(n) = p(p-1)^2(1-F(n-3)),$$

Consider the architecture of the 2. The result is treated as if it is the same with the previous result. To apply the result to the  $n$ -th cycle must be: the result of the last two) were correct; b) previous result was incorrect (otherwise the result would have been adopted in the previous cycle); the result was not accepted) to the  $(n-3)$  first cycles. Thus, where is the cumulative distribution function, which is equal to the probability of getting the correct result for  $n$  or less cycles.

LPI 3 using the majority of the element. The result will be adopted if it matches with at least one of the previous two. Note that this result cannot be simultaneously to two previous results, otherwise the result would have been adopted in the previous cycle. Let result was adopted at the  $n$ -th step and  $n > 4$ . Suppose that the current result is equal to the previous one. Then: a) at the  $n$ -th and  $(n-1)$ -th cycle was obtained the correct results; b)  $(n-2)$ -th and  $(n-3)$  third cycle were received incorrect results, otherwise the result would have been adopted in the previous cycle; c) for the first  $(n-4)$  loop result was not adopted.

$$P_3(n) = (1 - F(n - 4))(pq)^2 + (1 - F(n - 5))p(pq)^2, \text{ or}$$

$$P_3(n) = (1 - F(n - 4) + pF(n - 5))(pq)^2,$$

Suppose that the current result is obtained (n-2)-th cycle: a) at the n-th and (n-2)-th cycle was obtained the correct results; b) by (n-1)-th and (n-3)-th and (n-4)-cycles were received incorrect results, otherwise the result would be adopted at the (n-2)-th and (n-1)-th cycle; n) for the first (n-5) steps, the result was not adopted. Thus, the probability of a result on the n-th step  $n > 4$ :  $P_3(n) = (1 - F(n - 4))(pq)^2 + (1 - F(n - 5))p(pq)^2$ , or  $P_3(n) = (1 - F(n - 4) + pF(n - 5))(pq)^2$ , where is the cumulative distribution function, which is equal to the probability of getting the correct result for n or less cycles.

The average number of cycles (in fact the instructions), which is a single instruction for any architecture that is defined by the mathematical expectation the function  $P_i(n)$  appropriate architecture and directly depends on the likelihood of a in Fig. 1, 9, 10 are based on the average number of cycles (according to instructions) of error probability the original architecture with graphics 1, 2, architecture-retrofit using 3-element of the majority.

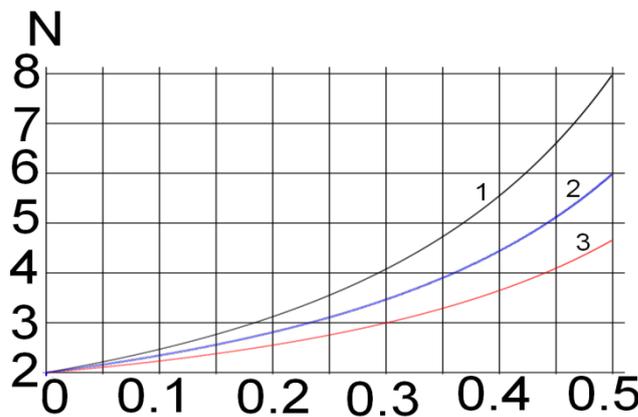


Fig. 9. Medium of cycles when  $p < 0,5$

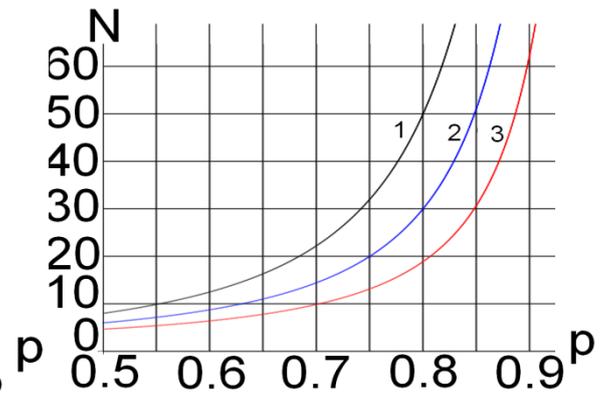


Fig. 10. Medium of cycles when  $p > 0,5$

As you can see from Figure 1 9, 10, when any error probability for 3 with the majority part of the average number of cycles (following the instructions) to obtain the result is minimal and the original architecture is as much as 1. In Fig. 1 11 shows the relative decrease in the average number of cycles (instructions) for the retrofit of architecture and architecture the majority element relative to the original architecture 1..

Obviously, to increase the speed of the system it is advisable to use the architecture of 3 with the majority element, but while using it, you must have an additional register, as well as, in case of an error, then copy the signature of what not to do when other types of architecture.

### Conclusions

In the analyzed the principles of construction noise defended processor architectures for modern computer systems. Describes the function and characteristics of modernization for the three architectures, showing their advantages and disadvantages are listed according to speed of work (number of

executable statements) of the probability calculation errors

#### LIST OF USED SOURCES

1. *Затуливетер Ю.С.* Разработка и исследование методов повышения надёжности распределенных вычислений / *Ю.С. Затуливетер, Е.А. Фищенко, И.А. Ходаковский* // Надёжность. – 2009. – Вып. 1. – С. 42–49.

2. *Матушевский В.В.* Вычислительные системы : учебное пособие / *В.В. Матушевский, Ю.А. Гунченко*. – Одесса : ВМВ, 2011. – 204 с.

3. Donald E. Steiss, Single event upset tolerant microprocessor architecture [Електронний ресурс]. – Режим доступа : <http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnethtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=6,571,363.PN.&OS=PN/6,571,363&RS=PN/6,571,363>.

4. *Гнеденко Б.В.* Курс теории вероятности : Издание шестое / *Б.В. Гнеденко*. – Москва : "Наука". – 448 с.

5. Пат 67752 Україна, МПК(2006.01) G06F 12/08. Пристрій підвищення завадостійкості систем з програмним управлінням / *Гунченко Ю.О., Мартинюк С.М., Ленков С.В., Омельченко О.С., Купрацевич А.В.* ; заявник і патентовласник Одеський національний університет ім. І.І. Мечникова. – № u 201107423 ; заявл. 14.06.2011 ; опубл. 12.03.2012, Бюл. № 5.

6. *Омельченко А.С.* Архитектура процессора для отказоустойчивых вычислительных систем / *А.С. Омельченко, И.В. Мигов, Ю.А. Гунченко* // Восьма Регіональна конференція студентів і молодих науковців. – 2011. – С. 17–18.

7. Пат 76984 Україна, МПК (2006.01) G06F 11/27. Відмовостійкий процесорний пристрій з підвищеною швидкодією / *Гунченко Ю.О., Ленков С.В., Кобозева А.А., Мартинюк С.М., Борисенко І.І.* ; заявник і патентовласник Одеський національний політехнічний університет. – № u 2012 07958 ; заявл. 27.06.2012 ; опубл. 25.01.2013, Бюл. № 2.

8. *Гунченко Ю.О.* Завадостійкий процесорний пристрій з підвищеною швидкодією / *Ю.О. Гунченко, А.С. Омельченко, О.А. Пенко* // Тези доповідей Третьої Міжнародної науково-практичної конференції «Методи та засоби кодування, захисту й ущільнення інформації». – 2011. – с. 42.